REMARKS

The Office Action mailed August 11, 2004, has been received and reviewed. Claims 1 through 30 are currently pending in the application. Claims 1 through 6, 13 through 16, 20 through 22, 26 through 28 and 30 stand rejected. Claims 7 through 12, 17 through 19, 23 through 25 and 29 have been objected to as being dependent upon rejected base claims, but the indication of allowable subject matter in such claims is noted with appreciation.

Applicant has amended claim 13 and respectfully requests reconsideration of the application in view of the arguments set forth hereinbelow.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 6,118,184 to Ishio et al.

Claims 1 through 6, 13, 26 through 28 and 30 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ishio et al. (U.S. Patent No. 6,118,184). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 1 through 6 and 13

Independent claim 1 is directed to a semiconductor device package comprising: a lead frame including a die paddle and a plurality of lead fingers; a first semiconductor die adhered to the die paddle, the first semiconductor die exhibiting a first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the first semiconductor die is electrically coupled to at least one lead finger of the plurality of lead fingers; and a second semiconductor die adhered to the die paddle, the second semiconductor die exhibiting a second size different from the first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the second semiconductor die is electrically coupled to the at

least one lead finger, *wherein the second semiconductor die exhibits circuitry substantially identical in function to circuitry of the first semiconductor die.*

The Examiner cites Ishio as disclosing: "a structure of a semiconductor device comprising a leadframe (see Fig. 2) including a die paddle 5 and a plurality of lead fingers 6; a first semiconductor die 1a adhered to the die paddle, the first semiconductor die 1a exhibiting a first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of [bond] pads of the semiconductor die 1a is electrically coupled to at least one lead finger of the plurality of lead fingers; and a second semiconductor die 1b adhered to the die paddle 5, the second semiconductor die 1b exhibiting a second size different from the first size (see column 6, lines 37-40) and having a plurality of [bond] pads, wherein at least one bond pad of the plurality of bond pads of the second semiconductor die 1b is electrically coupled to the at least one lead [finger], wherein the second semiconductor die 1b exhibits circuitry substantially identical in function to circuitry of the first semiconductor die 1a." (Office Action, page 2). Applicants respectfully disagree.

Ishio discloses a semiconductor device that includes two semiconductor chips 1a and 1b which are of different sizes. "Namely, the semiconductor chip 1b (second semiconductor chip) has a smaller element forming face area than the semiconductor chip 1a (first semiconductor chip)." (Col. 6, lines 45-48). However, beyond the comparative size of the semiconductor chips, Ishio does not appear to disclose specific details regarding such chips. More specifically, Applicants fail to find, and the Examiner fails to point to, any specific teaching by Ishio regarding the second semiconductor chip (1b) exhibiting circuitry substantially identical in function to the first semiconductor chip (1a). As such, Applicants submit that Ishio clearly does not anticipate claim 1 of the presently claimed invention.

Applicants further submit that claims 2 through 6 and 13 are also allowable over Ishio as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claims 3 and 13, Applicants submit that Ishio fails to teach a die paddle that exhibits a peripheral outline that is smaller than a peripheral outline of the first semiconductor die. While the size of Ishio's die paddle (5, 55) is not explicitly discussed with respect to comparing its peripheral outline with that of the semiconductor dies, the drawings

indicate that the peripheral outline of the die paddle is larger than each of those of the semiconductor dice.

Applicants, therefore, submit that claims 1 through 6 and 13 are in condition for allowance and respectfully request reconsideration and allowance thereof.

Claims 26 through 28 and 30

Independent claim 26 is directed to a method of forming a semiconductor device package. The method comprises: providing a lead frame having a die paddle and a plurality of lead fingers; providing a first semiconductor device exhibiting a first size; adhering a surface of the first semiconductor die to the die paddle; electrically connecting at least one of a plurality of bond pads formed on the first semiconductor die to a first lead finger of the plurality of lead fingers; providing a second semiconductor device exhibiting a second size different from the first size and *configuring circuitry of the second semiconductor die to be substantially identical in function to circuitry of the first semiconductor die*; adhering an active surface of the second semiconductor die to an upper side of the die paddle; and electrically connecting at least one of a plurality of bond pads formed on the active surface of the second semiconductor die to a second lead finger of the plurality of lead fingers.

As set forth hereinabove, Ishio discloses a semiconductor device that includes two semiconductor chips 1a and 1b which are of different sizes. "Namely, the semiconductor chip 1b (second semiconductor chip) has a smaller element forming face area than the semiconductor chip 1a (first semiconductor chip)." (Col. 6, lines 45-48). However, beyond the comparative size of the semiconductor chips, Ishio does not appear to disclose specific details regarding such chips. More specifically, Applicants fail to find, and the Examiner fails to point to, any specific teaching by Ishio regarding configuring the circuitry of the second semiconductor die to be substantially identical in function to the circuitry of the first semiconductor die. As such, Applicants submit that Ishio clearly does not anticipate claim 26 of the presently claimed invention.

Applicants further submit that claims 27, 28 and 30 are also allowable over Ishio as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claim 28, Applicants submit that Ishio fails to teach forming the die paddle with a peripheral outline which is smaller than a peripheral outline of the first semiconductor die.

Applicants, therefore, respectfully request reconsideration and allowance of claims 2 through 28 and 30.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,118,184 to Ishio et al. as applied to claims 1 through 6, 13, 26 through 28 and 30 and further in view of U.S. Patent No. 5,677,569 to Choi et al.

Claims 14 through 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishio et al. (U.S. Patent No. 6,118,184) as applied to claims 1 through 6, 13, 26 through 28 and 30 and further in view of Choi et al. (U.S. Patent No. 5,677,569). Applicant respectfully traverses this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
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> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of the claims are improper because the references relied upon by the Examiner fail to teach or suggest all of the limitations of the claims.

Independent claim 14 is directed to a memory device comprising: a carrier substrate; a plurality of electrical contacts coupled with electrical circuitry formed in the carrier substrate; and at least one semiconductor device package coupled with the electrical circuitry in the carrier substrate. The at least one semiconductor device package comprises: a lead frame including a die paddle and a plurality of lead fingers; a first semiconductor die adhered to the die paddle, the

first semiconductor die exhibiting a first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the first semiconductor die is electrically coupled to at least one lead finger of the plurality of lead fingers; and a second semiconductor die adhered to the die paddle, the second semiconductor die exhibiting a second size different from the first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the second semiconductor die is electrically coupled to the at least one lead finger, *wherein the second semiconductor die exhibits circuitry substantially identical in function to circuitry of the first semiconductor die.*

The Examiner relies on Ishio as applied to claims 1 through 6, 13, 26 through 28 and 30, and then cites Choi as disclosing "a memory device having a plurality of individual packages stacked over one another between upper and lower plates disposed on a carrier substrate (PCB)." (Office Action, pages 3-4). The Examiner then states that it would have been obvious to combine a carrier substrate, such as a PCB, as taught by Choi, with the package of Ishio.

As disclosed hereinabove, Ishio discloses a semiconductor device that includes two semiconductor chips 1a and 1b which are of different sizes. "Namely, the semiconductor chip 1b (second semiconductor chip) has a smaller element forming face area than the semiconductor chip 1a (first semiconductor chip)." (Col. 6, lines 45-48). However, beyond the comparative size of the semiconductor chips, Ishio does not appear to disclose specific details regarding such chips. More specifically, Applicants fail to find, and the Examiner fails to point to, any specific teaching by Ishio regarding the second semiconductor chip (1b) exhibiting circuitry substantially identical in function to the first semiconductor chip (1a). Nor does Choi appear to teach or suggest such subject matter.

Applicants, therefore, submit that claim 14 is allowable over Ishio and Choi. Applicants further submit that claims 15 and 16 are also allowable over Ishio at least by virtue of their dependency from an allowable base claim.

Applicants respectfully request reconsideration and allowance of claims 14 through 16.

Obviousness Rejection Based on U.S. Patent No. 6,118,184 to Ishio et al. as applied to claims 1 through 6, 13, 26 through 28 and 30 and further in view of U.S. Patent No. 6,707,684 to Andric et al.

Claims 20 through 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishio et al. (U.S. Patent No. 6,118,184) as applied to claims 1 through 6, 13, 26 through 28 and 30 and further in view of Andric et al. (U.S. Patent No. 6,707,684). Applicant respectfully traverses this rejection, as hereinafter set forth.

Independent claim 20 is directed to a computing system comprising: a carrier substrate; a processor operably coupled to the carrier substrate; at least one input device operably coupled with the carrier substrate; at least one output device operably coupled with the carrier substrate; and a memory device operably coupled to the carrier substrate, the memory device including at least one semiconductor device package. The at least one semiconductor device package comprises: a lead frame including a die paddle and a plurality of lead fingers; a first semiconductor die adhered to the die paddle, the first semiconductor die exhibiting a first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the first semiconductor die is electrically coupled to at least one lead finger of the plurality of lead fingers; and a second semiconductor die adhered to the die paddle, the second semiconductor die exhibiting a second size different from the first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the second semiconductor die is electrically coupled to the at least one lead finger, *wherein the second semiconductor die exhibits circuitry substantially identical in function to circuitry of the first semiconductor die.*

The Examiner relies on Ishio as applied to claim 1, and then cites Andric as disclosing personal computer systems having a processor mounted in a socket that is commonly mounted to a PCB. (See, Office Action, page 4). The Examiner then states that "it would have been obvious to a person of ordinary skill in the pertinent art to couple the processor to the carrier substrate such as PCB [sic], as is notoriously known." (Office Action, page 5).

As disclosed hereinabove, Ishio discloses a semiconductor device that includes two semiconductor chips 1a and 1b which are of different sizes. "Namely, the semiconductor chip 1b (second semiconductor chip) has a smaller element forming face area than the semiconductor

chip 1a (first semiconductor chip)." (Col. 6, lines 45-48). However, beyond the comparative size of the semiconductor chips, Ishio does not appear to disclose specific details regarding such chips. More specifically, Applicants fail to find, and the Examiner fails to point to, any specific teaching by Ishio regarding the second semiconductor chip (1b) exhibiting circuitry substantially identical in function to the first semiconductor chip (1a). Nor does Andric appear to teach or suggest such subject matter.

Applicants, therefore, submit that claim 14 is allowable over Ishio and Choi. Applicants further submit that claims 15 and 16 are also allowable over Ishio at least by virtue of their dependency from an allowable base claim.

Applicants respectfully request reconsideration and allowance of claims 14 through 16.

Objections to Claims/Allowable Subject Matter

Claims 7 through 12, 17 through 19, 23 through 25 and 29 stand objected to as being dependent upon rejected base claims, but are indicated to contain allowable subject matter and would be allowable if placed in appropriate independent form.

As set forth hereinabove, Applicants submit that claims 1 (from which claims 7 through 12 depend), 14 (from which claims 17 through 19 depend), 20 (from which claims 23 through 25 depend) and 26 (from which claim 29 depends) are each in condition for allowance. Applicants, therefore submit that claims 7 through 12, 17 through 19, 23 through 25 and 29 are also in condition from allowance and respectfully requests reconsideration thereof.

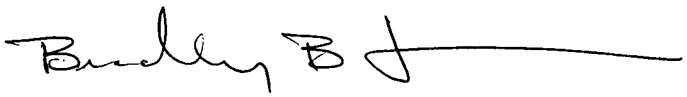
ENTRY OF AMENDMENTS

The amendment to claim 13 above should be entered by the Examiner because the amendment is supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search.

CONCLUSION

Claims 1 through 30 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



Bradley B. Jensen
Registration No. 46,801
Attorney for Applicant
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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